UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,449	12/10/2001	Robert Thomas Bailis	RPS920010127US1	5286

47052 7590 01/17/2008

SAWYER LAW GROUP LLP
PO BOX 51418
PALO ALTO, CA 94303

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
01/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent@sawyerlawgroup.com
nikia@sawyerlawgroup.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT THOMAS BAILIS, CHARLES EDWARD KUHLMANN, CHARLES STEVEN LINGAFELT, and ANN MARIE RINCON

Appeal 2007-2531
Application 10/016,449
Technology Center 2100

Decided: January 15, 2008

Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and ALLEN R. MACDONALD, *Administrative Patent Judges*.

MACDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal a Final Rejection of claims 1-9, 12, 14, and 15 under 35 U.S.C. § 134. We have jurisdiction under 35 U.S.C. § 6(b).

According to Appellants, they invented a debug function that debugs logic functions of an application specific integrated circuit (ASIC).

(Spec. 3:6-18.) The debug function includes: (1) a comparator that compares signals from the logic functions with a trigger pattern downloaded from a server and (2) storage logic that stores the signals that match the trigger pattern for later retrieval by the server. (Spec. 5:20-7:15.)

Claim 1 is exemplary and is reproduced below:

1. An application specific integrated circuit (ASIC) comprising:

a standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) coupled to the at least one bus and the plurality of internal signals, the field programmable gate array (FPGA) including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals, the debug client function being in communication with a server and including,

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Shen	US 6,829,751 B1	Dec. 7, 2004 (filed Oct. 6, 2000)

Claims 1-9, 12, and 14-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen.

We affirm.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Shen

1. Shen teaches that debugging workstation 104 can be "configured to detect errors in the logic portion through the one or more interfaces." (Col. 2, ll. 63-65.)
2. Shen teaches that "FPGA core 116 can also be used to add or verify bug fixes." (Col. 6, ll. 52-53.) Shen also teaches that workstation 104 is used to program FPGA core 116 to support many debugging features such as "programmed *triggering and tracing based on internal signals*" and "complex monitoring functions (e.g., protocol monitoring)." (Col. 5, ll. 18-19 and Col. 6, ll. 32-42 (emphasis added)).
3. Shen teaches that a "user can easily decide *which signals need to be observed* during the debugging period" (col. 5, ll. 32-33 (emphasis

added)) and "programing the FPGA core to implement user required functions" (col. 5, ll. 18-19).

4. Shen teaches that FPGA core 116 is "to *collect* data from the registers 120a-120n and 122a-122n" (emphasis added) (col. 3, ll. 37-40) and "only the data from the registers that needs to be *monitored* may be stored and compressed. The I/O [input/output] interface may then transfer the data to the debugging workstation 104" (emphasis added) (col. 4, ll. 55-58). Shen teaches "[a]fter the data is collected and compressed, the data will be sent to the debugging workstation 104" (col. 3, ll. 52-53) and "waveforms of the internal signals under probing can be displayed as if they are directly connected to a logic analyzer by internal wires" (col. 3, ll. 54-57).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls."). The Court in *Graham* further noted that evidence of secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18. "If a court, or patent examiner, conducts this analysis and concludes the claimed subject matter was obvious, the claim is invalid under § 103." *KSR*, 127 S. Ct. at 1734.

The Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248 [(1850)]." *KSR,* 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)), and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."

Id. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740. "[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *Id.* (citing *Sakraida v. AG Pro, Inc.*, 425 U. S. 273, 282 (1976)).

ANALYSIS

Claim 1

The Examiner concludes that Shen teaches all elements of claim 1. (Ans. 3-4 and 7-11.) Appellants allege that Shen fails to teach a debug client function and more specifically that Shen fails to teach a "comparator logic" that is "operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server" and also fails to teach "storage logic" that is "operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server." (App. Br. 4-6.)

Therefore the issues are whether the Appellants have shown that the Examiner erred by finding that Shen teaches the comparator logic and the storage logic.

Comparator Logic

Appellants allege that Shen does not teach functions of monitoring, verifying bug fixes, and detecting errors contained *within* FPGA core 116 but rather that the functions are performed *external* to the FPGA core 116 at debugging workstation 104. (App. Br. 5 and Reply Br. 2-3.) Shen teaches multiple embodiments: an external debugging embodiment performs debugging within debugging workstation 104 (FF 1) whereas an internal debugging embodiment performs debugging within FGPA core 116 (FF 2). Shen's internal debugging embodiment teaches using debug workstation 104 to program the FPGA core 116 to identify received signals that match a programmed triggering signal pattern. (FF 2.) Likewise, the claimed comparator logic requires comparing selected internal signals coupled to the FPGA with a trigger pattern downloaded from the server. Thus, both Shen's internal debugging embodiment and the comparator logic involve determining whether signals received by an FPGA match a pattern prescribed by a computer. Accordingly, Shen's internal debugging embodiment teaches the claimed comparator logic.

Appellants allege that the external debugging embodiment teaches away from the internal debugging embodiment. (App. Br. 5-6 and Reply Br. 3.) However, Shen's teaching of multiple embodiments did not teach away from any particular embodiment. The external debugging embodiment of Shen provides an alternative approach but does not discourage use of the internal debugging embodiment. *See Para-Ordnance Mfg. v. SGS Importers*

Int'l, 73 F.3d 1085, 1090 (Fed. Cir. 1995) (the Browning Hi-Power handgun does not teach away from the claimed invention; while it fails to disclose a converging frame, it does not warn a person against using convergence); *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) ("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.").

Thus, Appellants have failed to show that the Examiner erred by finding that Shen teaches the claimed comparator logic.

Storage Logic

Appellants allege that Shen's FPGA core 116 stores signals that are "pre-selected by a user," but Shen's FPGA core 116 does not store signals that match a trigger pattern. (App. Br. 6.) In addition, Appellants allege that FPGA core 116 cannot store signals that match a trigger pattern that is later retrieved by the server because Shen does not teach specifically how FPGA core 116 searches for a signal pattern that matches a trigger pattern. (*Id.*).

The claimed storage logic requires storing signals that match a trigger pattern for later retrieval by the server. We agree with the Examiner (Ans. 4 and 11) that Shen's teachings of (1) user deciding *which signals need to be observed* during the debugging period (FF 3), (2) programming FPGA core 116 to implement user required functions (FF 3), and (3) FPGA core 116

transfers selected internal signals to workstation 104 (FF 4) teaches that the FPGA core 116 stores signals that match a prescribed pattern for later retrieval by workstation 104. Accordingly, we find that Shen teaches the requirements of the claimed storage logic.

Alternatively, we find that Shen's teachings of (1) FPGA 116 collecting data from registers that need to be monitored (FF 4) and (2) transferring the data to workstation 104 (FF 4) teach that FPGA core 116 stores signals that match a prescribed signal pattern and transfers the signals to workstation 104. Thereby, Shen's teachings meet all requirements of the claimed storage logic.

We note that the Examiner applies teachings from the internal and external debugging embodiments discussed *supra* to teach the respective comparator logic and storage logic. However, where, as here, "when a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR,* 127 S. Ct. at 1740 (citing *Sakraida*, 425 U. S. at 282). At the time of the invention, combining the internal debugging embodiment's FPGA core 116 that compares signals from register blocks 120a-120n with a signal pattern prescribed by workstation 104 with the external debugging embodiment's FPGA core 116 stores signals that match a pattern for retrieval by workstation 104 changed the functions of neither the internal nor external debugging embodiments because both performed the same operations, i.e.,

comparing signals with a pattern and storing the pattern for retrieval by a server. In addition, permitting access by a server of the signal pattern that matches the trigger pattern yields no more than an expected result.

In addition, Shen's external debugging environment provides a reason to combine the external debugging embodiment's storing signals that match a pattern for retrieval by workstation 104 with the internal debugging embodiment's comparing signals from register blocks 120a-120n with a signal pattern by teaching permitting a user to view waveforms of collected data. (FF 4.)

Therefore, we find that Appellants have failed to show that the Examiner erred in finding that Shen teaches the storage logic.

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a).

Claims 2-9, 12, and 14-15

Claims in this group are subject to the same rejection as claim 1. Appellants have not presented any substantive arguments directed to the separate patentability of claims in this group, but rely instead on arguments for patentability of claim 1. (App. Br. 6-7.) Therefore, as to the rejection of the claims in this group, Appellants have not shown Examiner error for the same reasons discussed *supra* with respect to claim 1.

CONCLUSION OF LAW

We conclude that:

(1) Appellants have not shown that the Examiner erred in concluding that Claims 1-9, 12, and 14-15 are unpatentable over Shen under 35 U.S.C. § 103(a); and

(2) Claims 1-9, 12, and 14-15 are not patentable.

DECISION

The Examiner's rejection of claims 1-9, 12, and 14-15 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

SAWYER LAW GROUP LLP
P.O. BOX 51418
PALO ALTO CA 94303